

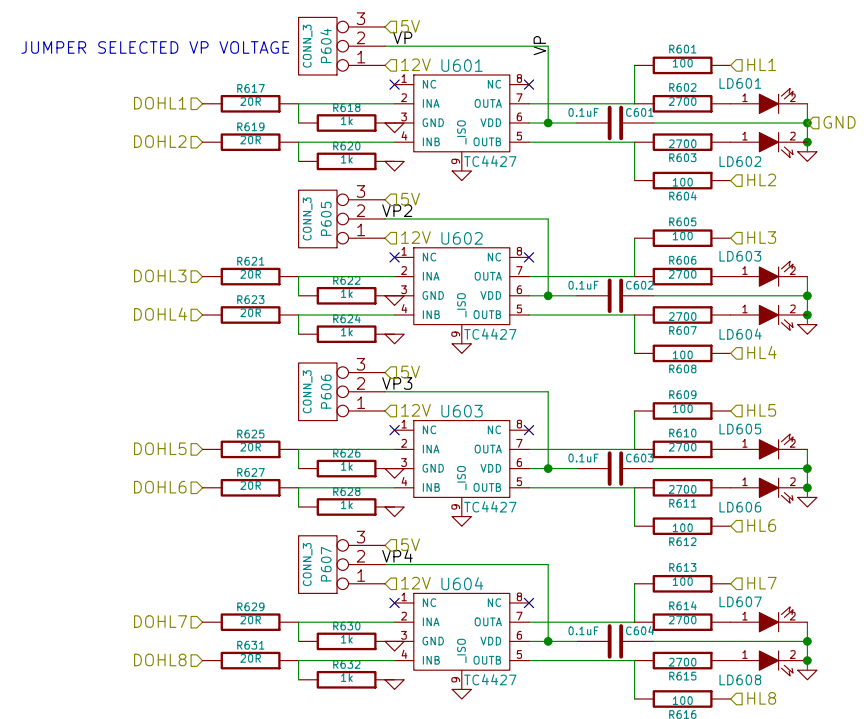
optional D12-D23 for solenoids
 only used in rare cases where the
 topology (IAC, VVT, ALT, ect) requires
 this fly back diode

rusEfi

The JP1 jumper is needed because we cannot feed the screen via USB - we would need to disconnect it while the board is on a bench

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Sheet: /	
File: frankenso.sch	
Title: frankenso	
Size: B	Date: 2018-02-24
KiCad E.D.A.	kiCad 4.0.5
Rev: 0.5.3	Id: 1/15

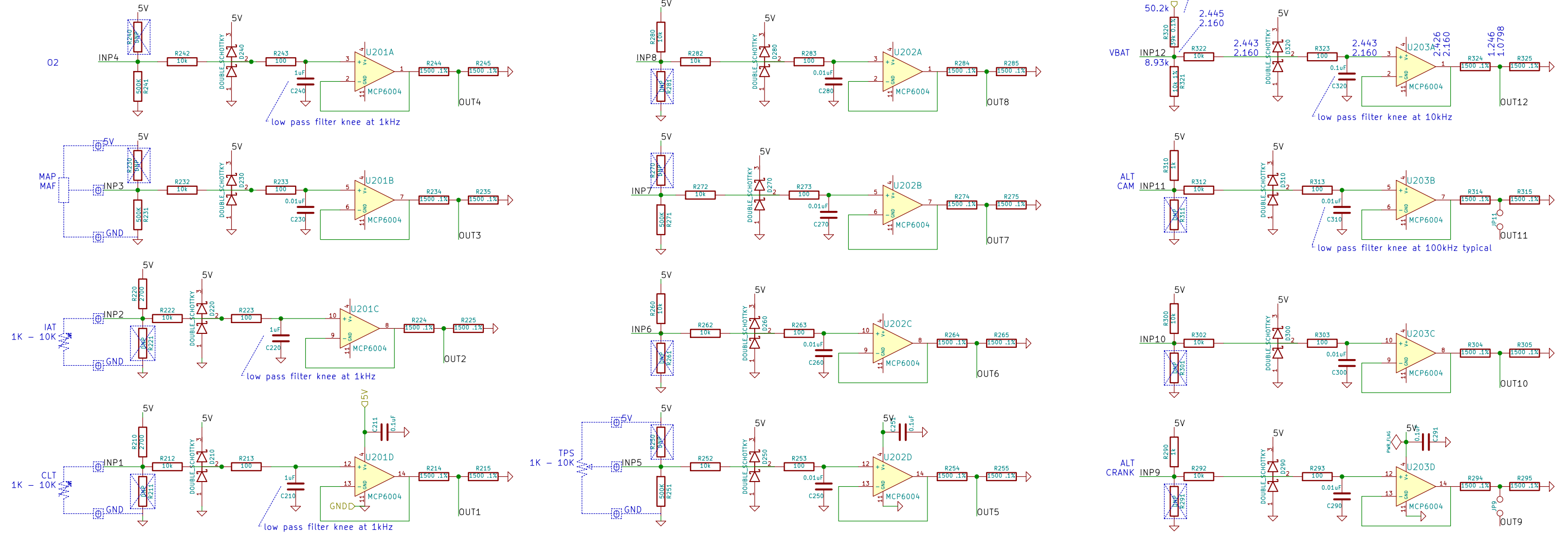
8 channel high / low side driver

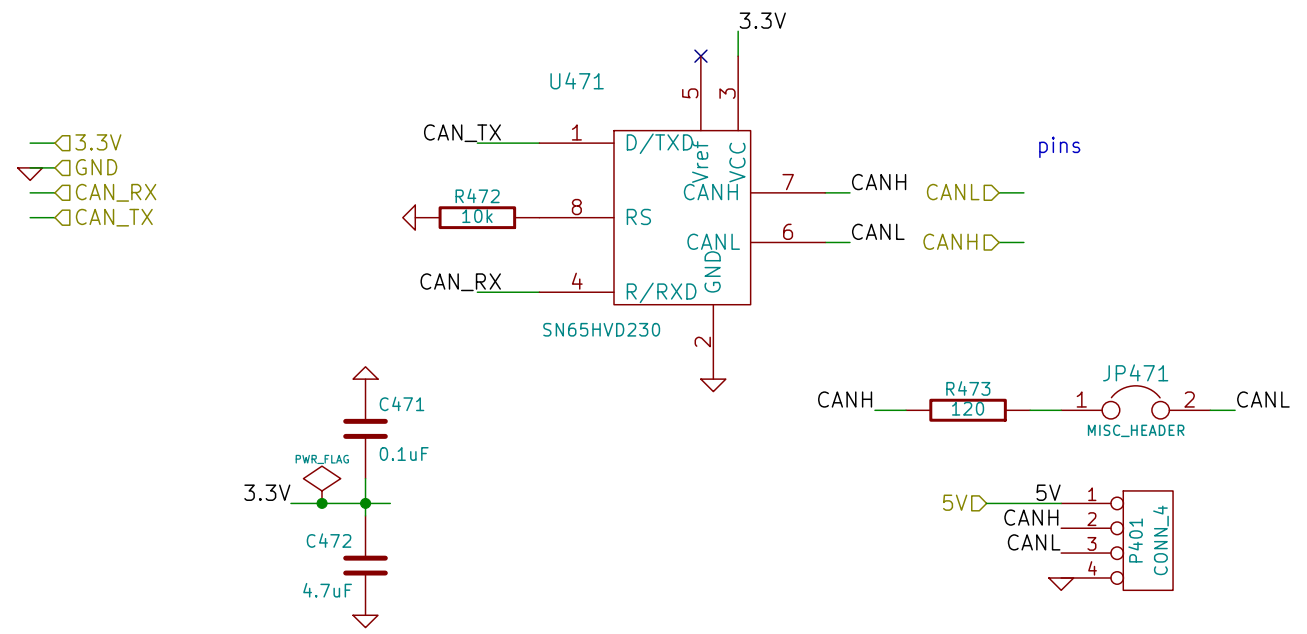


- INP12
- INP11
- INP10
- INP9
- INP8
- INP7
- INP6
- INP5
- INP4
- INP3
- INP2
- INP1

- OUT4
- OUT3
- OUT1
- OUT2
- OUT10
- OUT12
- OUT6
- OUT5
- OUT8
- OUT7
- OUT9
- OUT11

SUGGESTED / DEFAULT ENGINE WIRING IN BLUE

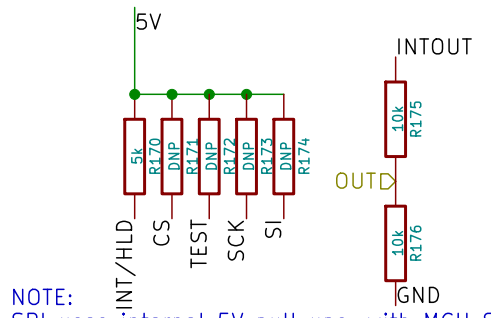
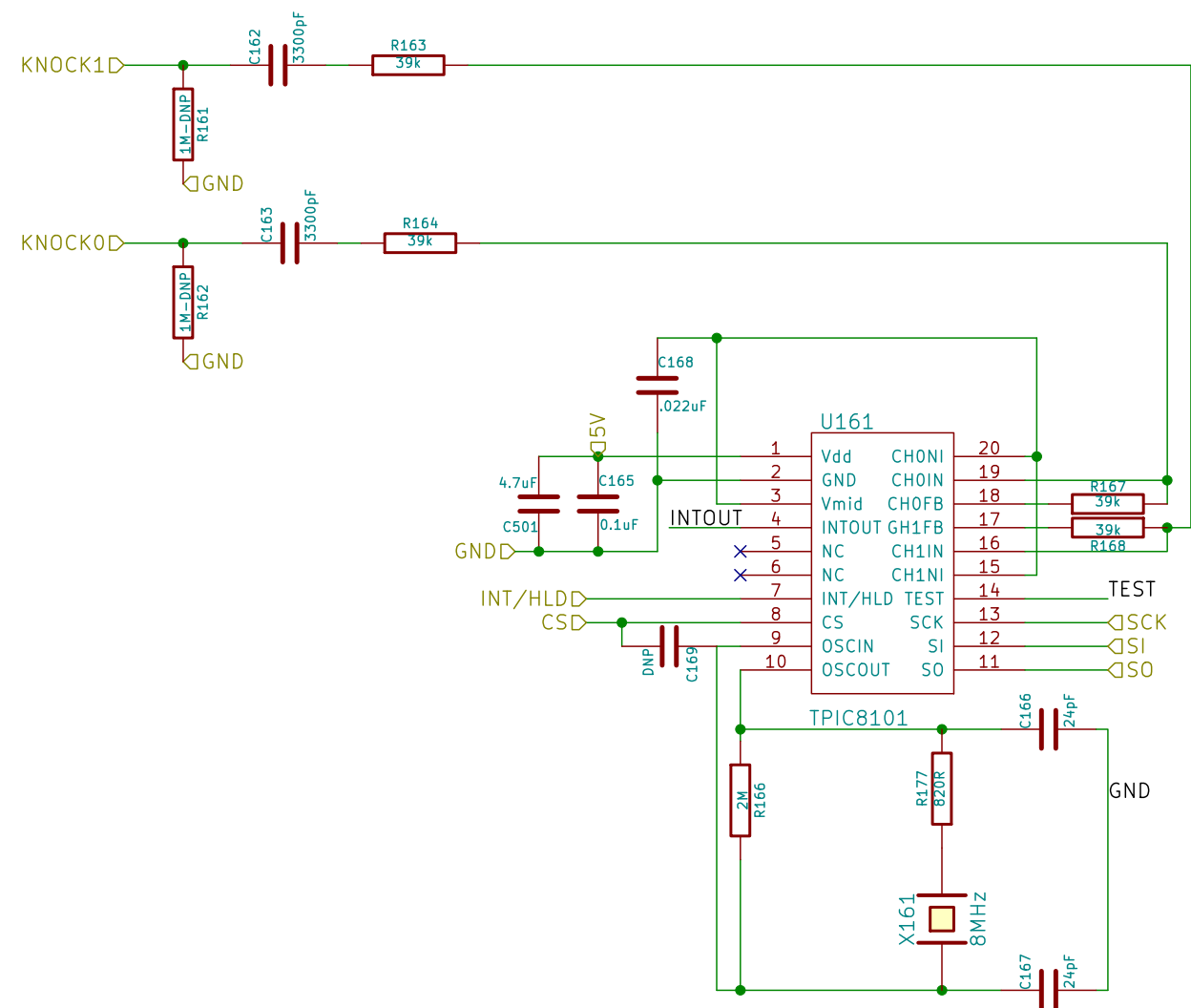




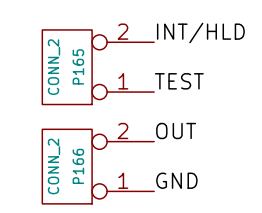
CAN level shifter

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Size: A	Date: 2018-02-24	Rev: 0.5.3
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DD_HIP9011 ver.2
RusEfi.com



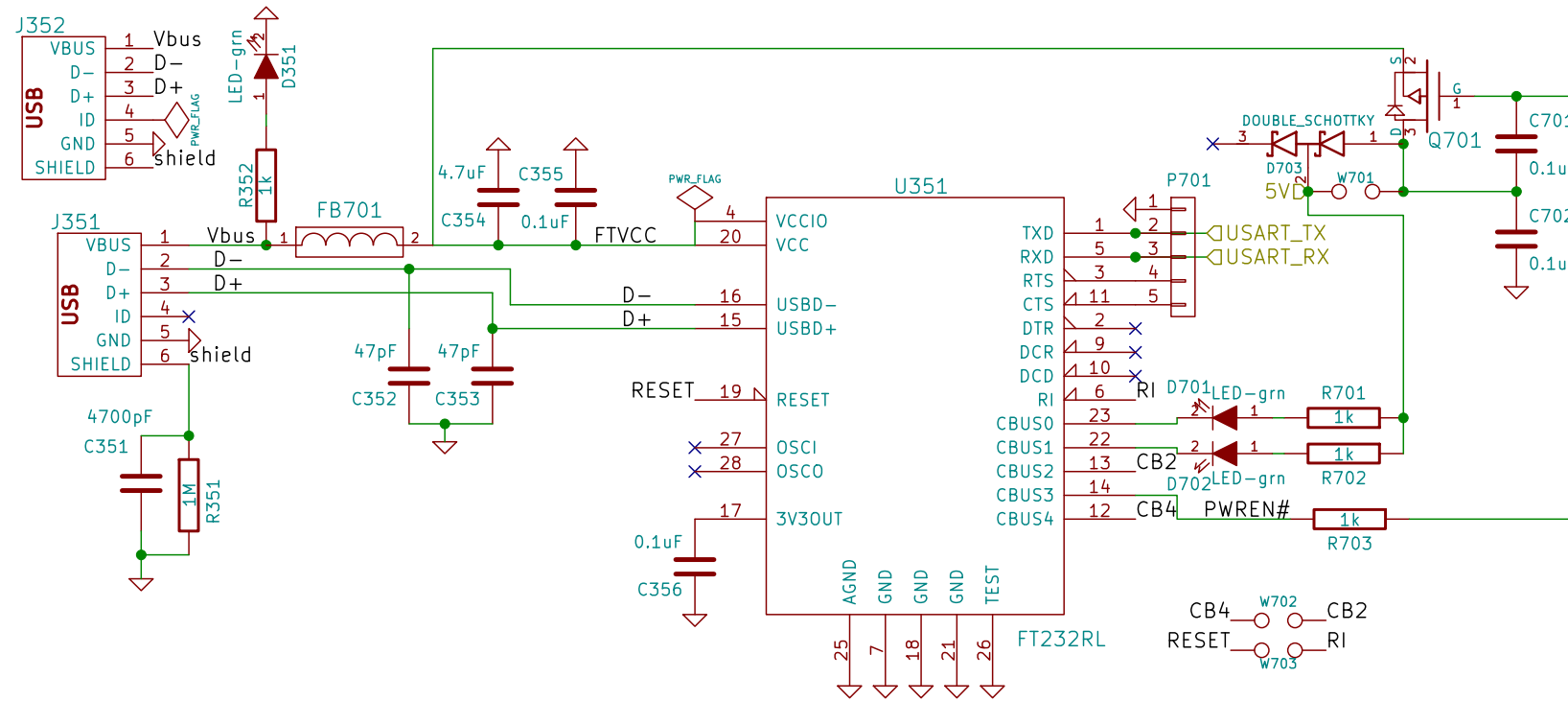
NOTE:
SPI uses internal 5V pull ups, with MCU SPI being float to pull down.
This allows 3.3V / 5V tolerate MCU's to use these SPI coms.



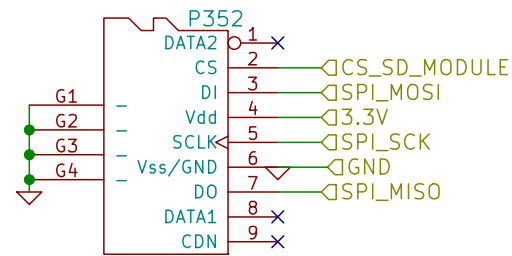
<http://www.crystek.com/documents/appnotes/Pierce-GateIntroduction.pdf>
PCB per predictions with SaturnPCB has less then 3.5pF traces,
TPIC pins assumed 5pF
ESR = 80ohms max
Rf = 2meg could be between 1meg and 10meg.
Cload should be 18pF per XTAL datasheet
Cload = ((Cin+C1)[C2+Cout])/(Cin+C1+C2_Cout)+PCBstray
Cload = ((5+24)[24+5])/(5+24+24+5)+3.5 = 18.0pF
C1=C2=C166=C167 = 24pF
Rs = 1/(2piFC2) = 1/(2*pi*8MHz*24pF) = 829ohms, 820ohms is close enough = R177

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Sheet: /DD_HIP9011/		
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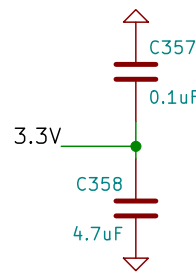
JUMPER WJ01 IS A BACKUP PLAN. THE VOLTAGE DROP ACROSS D703 MAY BE NOT TOLERABLE, SO WE HAVE A BACK UP PLAN IF WE NEED TO BYPASS THE DIODE WITH A LOWER VOLTAGE DROP



For right conn



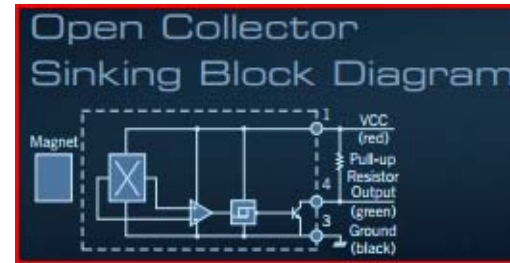
SD card slot
USB TTL module



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Size: A	Date: 2018-02-24	Rev: 0.5.3
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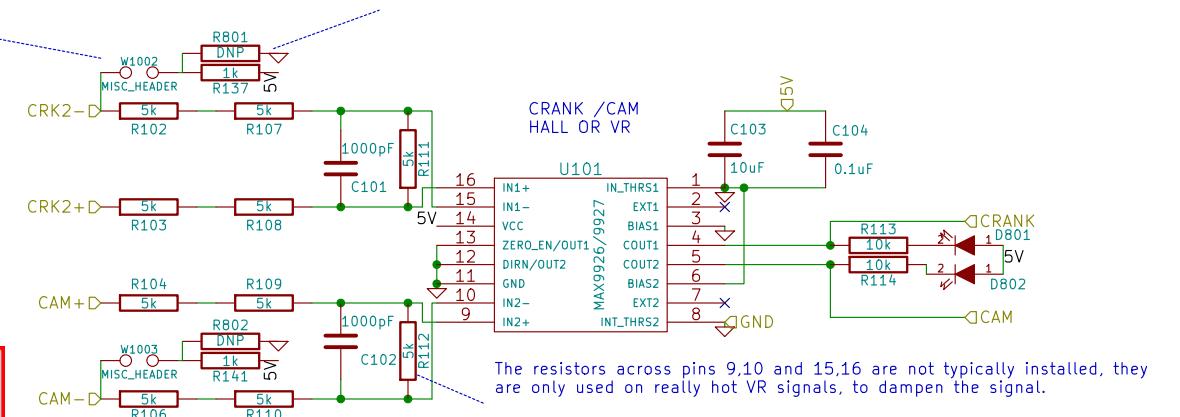
When configured for VR, DNP W1002 or W1003.
 These jumpers allow isolation which prevents the VR signal from getting into the 5V or GND.

Many Hall sensors are set as an open collector sinking topology. Those setups require a pull up resistor, and 1k ohm is a common size. These pull up resistors are noted as R137 and R141 on this page. You need to match these pull up resistors with your hall sensors requirements. Often you need about 5mA of drive. See snippet from Cherry hall sensors to the right. Some sensors are the inverse, and need a pull down resistor. These are less common. These pull down resistors are noted as R801 and R802 on this page and are not typically installed.



Recommended pull-up resistor values are as follows:

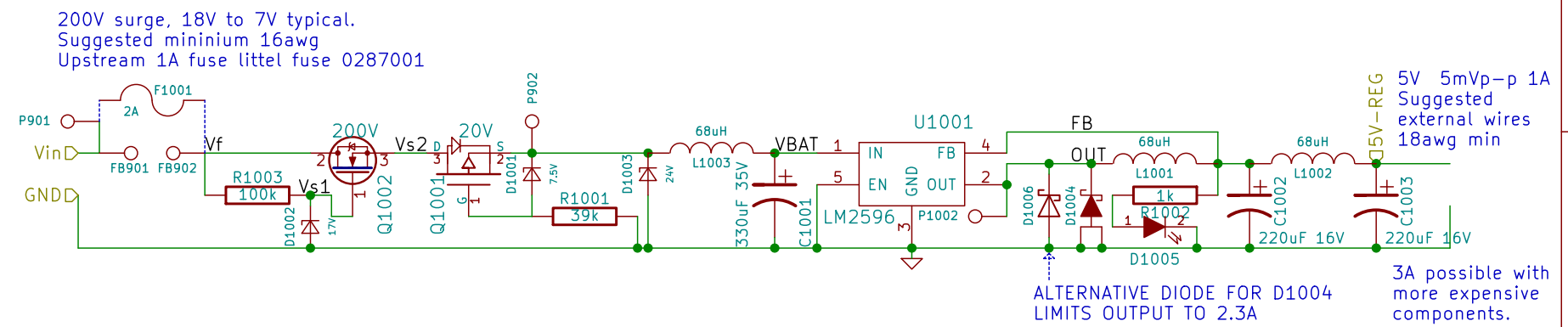
Volts dc	5	9	12	15	24
Ohms	1 k	1.8k	2.4 k	3 k	3 k



The resistors across pins 9,10 and 15,16 are not typically installed, they are only used on really hot VR signals, to dampen the signal.

Brief overview

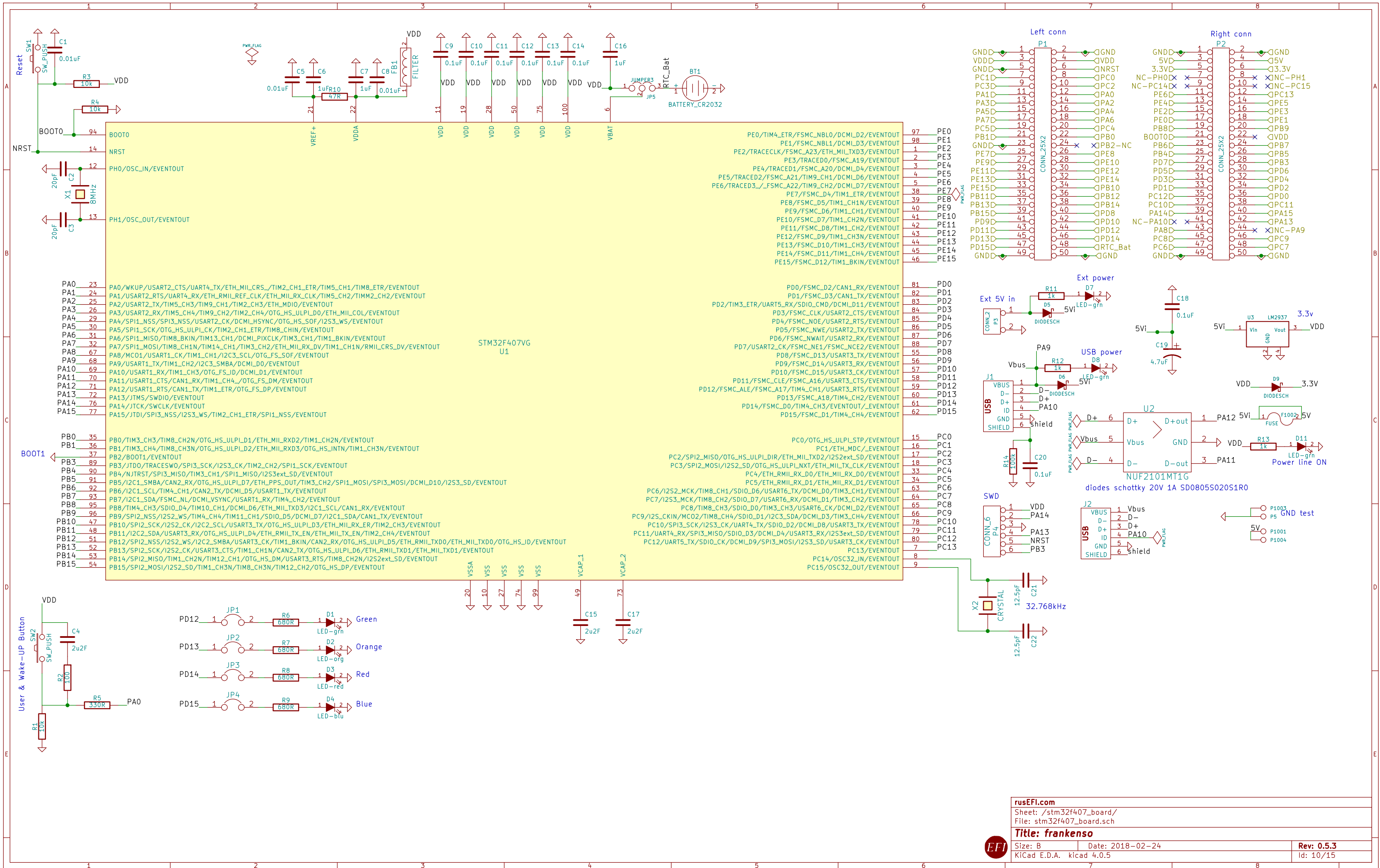
- Q1002, R1003, D1002 preform an active transient protection. It will suppress voltages up to 200V down to 19V.
 - Q1001, R1001, D1001 preform a reverse polarity protection. If the input signal is the wrong polarity, the gate will not conduct which will prevent current from flowing.
 - D1003 is a second transient suppressor, it would catch faster transients allowing a brief amount of time for Q1002 to preform it's duty.
 - L1003 is a choke, it simple prevents switching noise from going up the power wire where it can get into other circuits.
 - C1001 is a bulk cap, it simply stores energy locally such that the regulator can draw large currents in short periods of time.
 - U1001 and the components to the right, are a buck style switching regulator, that will pull the 5V line up to 5V. It will not pull it down from 5V if there is an external voltage.
- The U1001 circuit has been designed for 3A output and up to 20V input, but typically 14.4V or 12.4V input. L1001 wants to be about 68uH to 100uH with less than 0.3 ohms resistance.

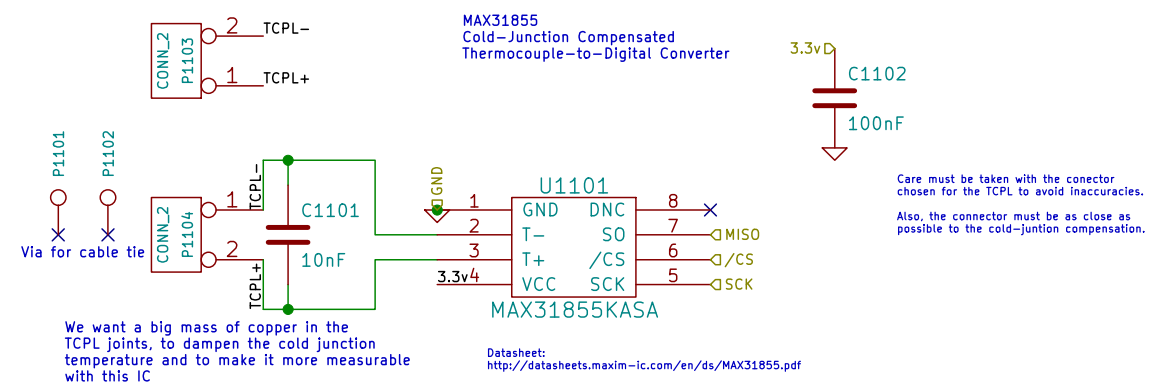


Alternate options

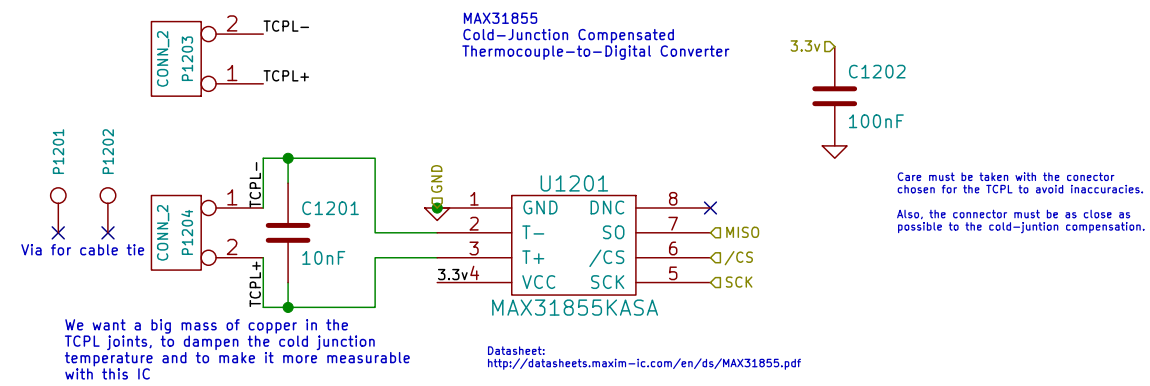
- Q1002 Microchip, DN2625K4-G with FAIRCHILD, 1N5247B
- D1002 IXYS, IXTA6N50D2 with FAIRCHILD, 1N5244B
- D1004 VISHAY, VS-50WQ04FN-M3 with VISHAY, VS-50WQ04FNPBF

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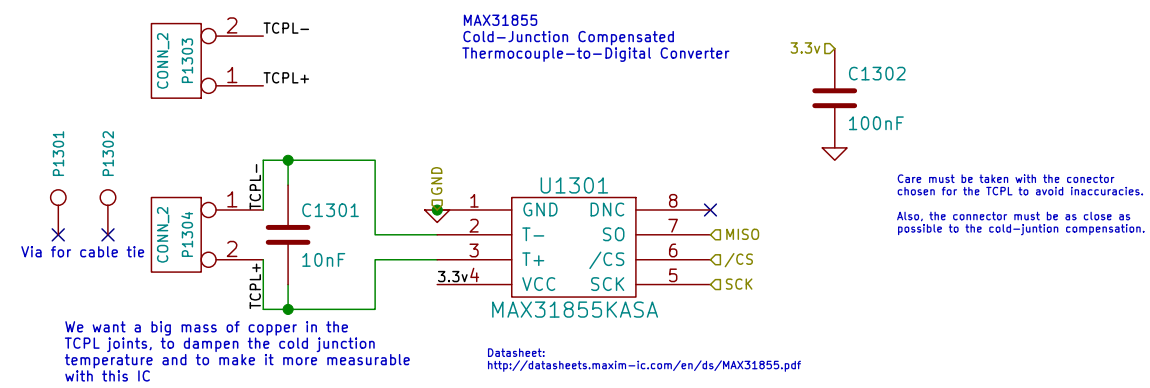
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Size: A Date: 2018-02-24

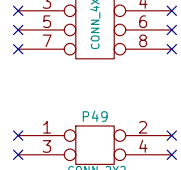
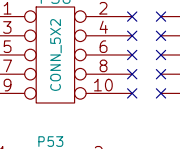
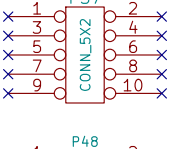
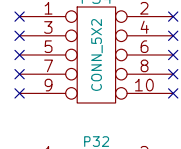
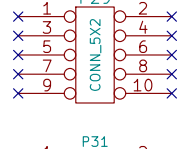
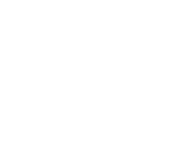
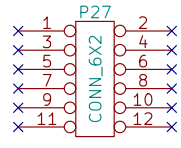
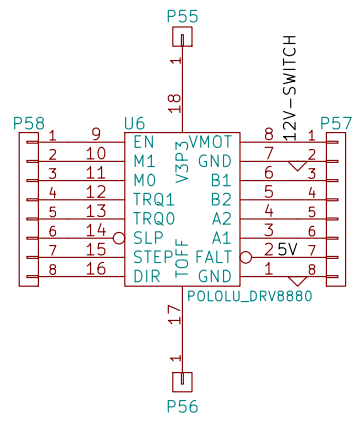
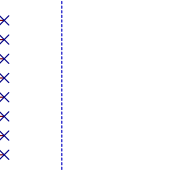
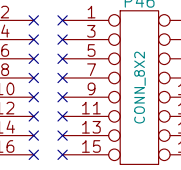
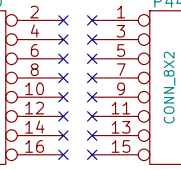
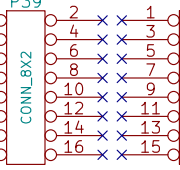
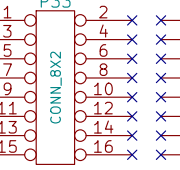
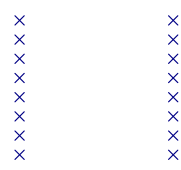
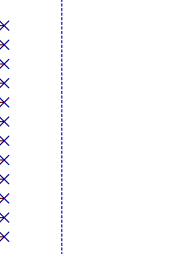
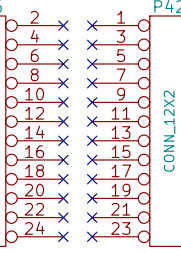
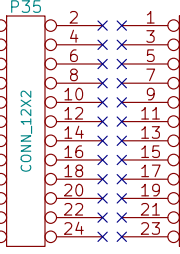
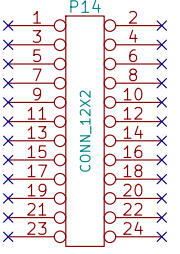
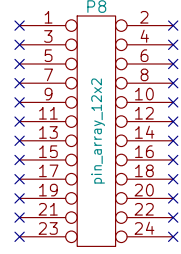
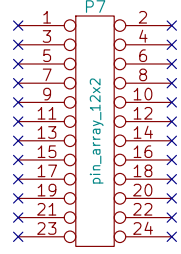
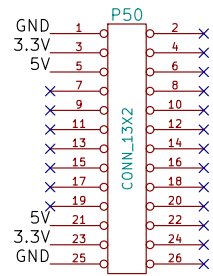
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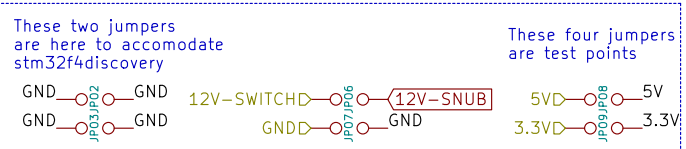
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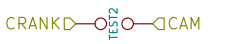
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PROTO AREA



That's alternative signal OUTPUT – these traces should be routable to PC6 and PA5 via jumpers. Alternative to W212 and W212 routing of op-amps ch 11 and ch 12



See below links about barriers in GND planes. The current loops in the layout do not appear to need barriers.

http://rusefi.com/wiki/index.php?title=Manual:Hardware:PCB_design_rules

<http://www.maximintegrated.com/en/app-notes/index.mvp/id/5450>

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