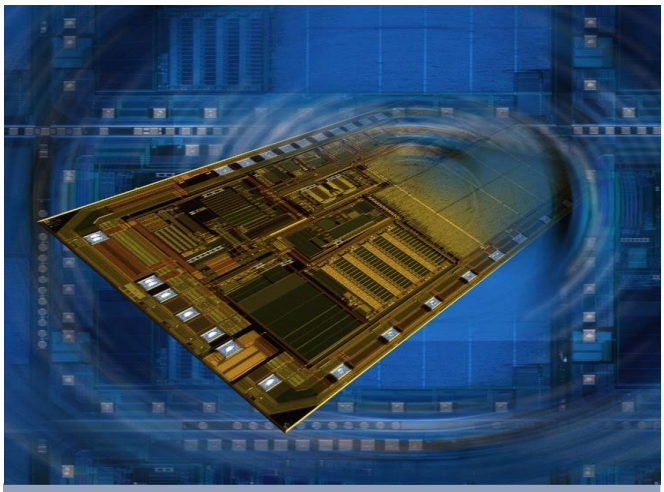
Automotive Electronics

# Product Information
# Engine Management IC - CJ945C

BOSCH
Invented for life



**18 fold power lowside switch with serial peripheral interface (SPI) and diagnostic functions**

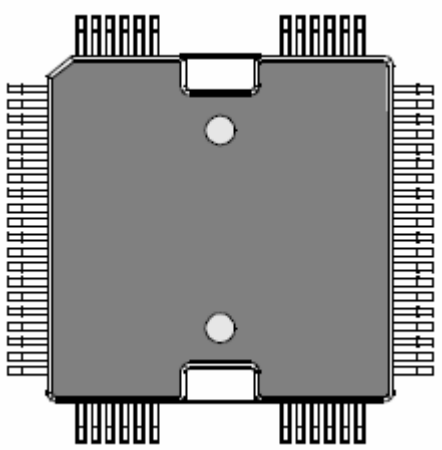
**Customer benefits:**

- Excellent system know-how
- Smart concepts for system safety
- Secured supply
- Long- term availability of manufacturing processes and products
- QS9000 and ISO/TS16949 certified

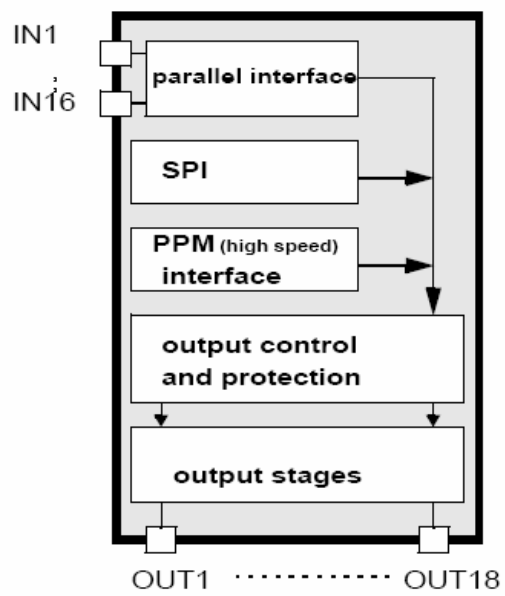
**Features**

- 4 relay drivers (... 1.1A)
- 6 valve drivers (... 2.2A)
- 2 valve drivers (....3.0A)
- 6 injection valve drivers (... 2.2A)
- SPI Interface
- PPM Interface (high speed interface, µs-Bus)
- Diagnostic features
- Internal short circuit protection
- Parallel connection of power stages possible
- Package: HiQUAD 64

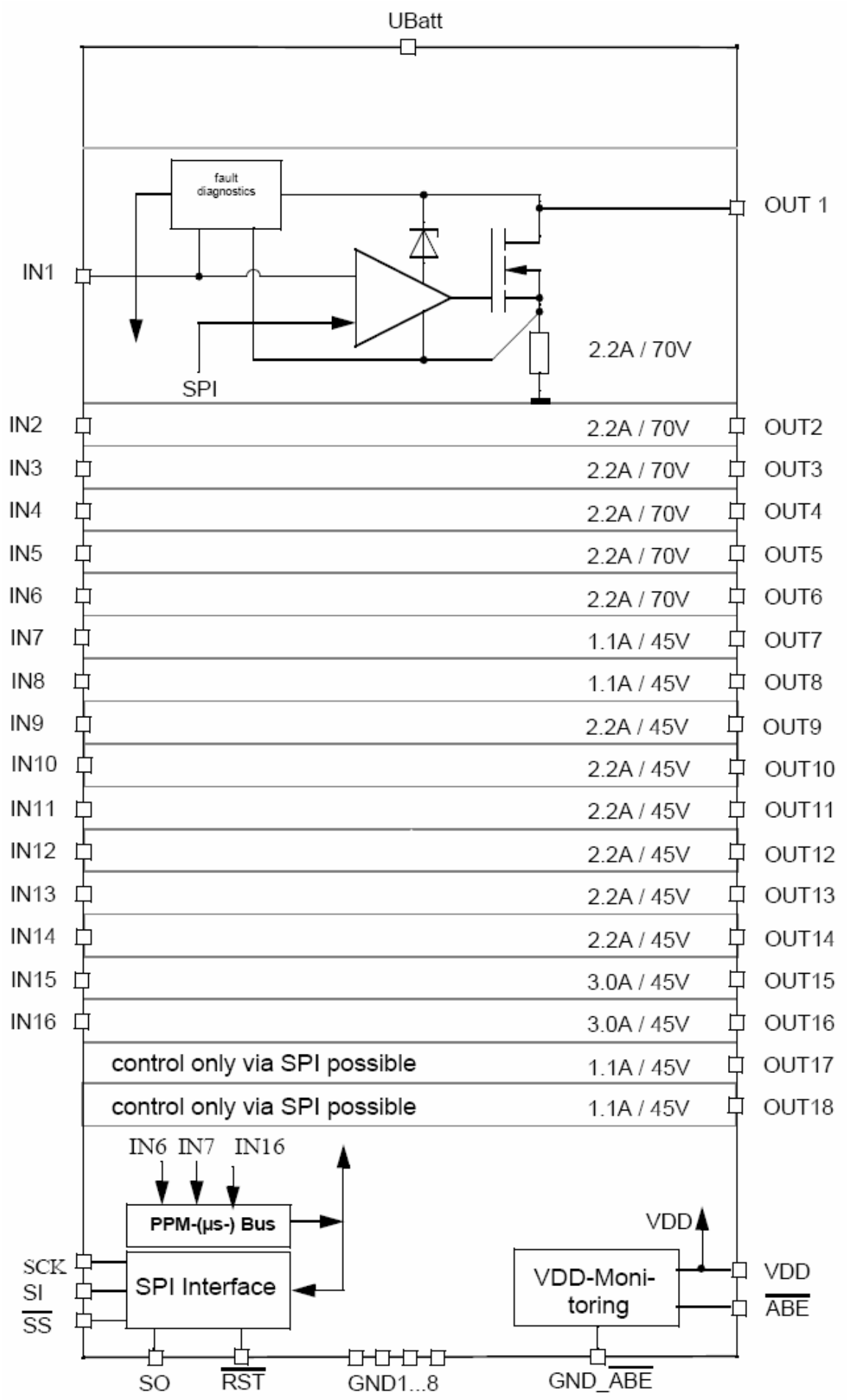
**PIN configuration**



HiQUAD64



## Block diagram



## Description power stages

### OUT1 ... OUT6

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the PPM-bus (ms-bus) or via SPI. For TJ = 25°C the on-resistance of the power switches is below 500mW.
An integrated zener diode limits the output voltage to 70V typically.
A protection for inverse current is implemented for OUT1... OUT4 in case of use as stepper motor control.

### OUT9 ... OUT14

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the PPM-bus (ms-bus) or via SPI. For TJ = 25°C the on-resistance of the power switches is below 450mW.
An integrated zener diode limits the output voltage to 45V typically.

### OUT15, OUT16

2 non-inverting low side power switches for nominal currents up to 3.0A. Control is possible by input pins, by the PPM-bus (ms-bus) or via SPI. For TJ = 25°C the on-resistance of the power switches is below 350mW.
An integrated zener diode limits the output voltage to 45V typically.

### OUT7, OUT8, OUT17, OUT18

4 low side power switches for nominal currents up to 1.1A. Stage 7 is non-inverting, stage 8 is inverting (IN8 = '1' => OUT8 is active). For the output OUT7 control is possible by the input pin, by the PPM-bus (ms-bus) or via SPI, OUT8 is controlled by the input pin IN8 or via SPI, for the outputs OUT17 and OUT18 control is only possible via SPI. For TJ = 25°C the on-resistance of the power switches is below 1000mW.
An integrated zener diode limits the output voltage to 45V typically.
In order to increase the switching current or to reduce the power dissipation, parallel connection of power stages is possible.

## The power stages are short-circuit proof:

### Power stages OUT1...OUT8, OUT11..OUT14:

In case of overload (SCB) they will be turned off after a given delay time. During this delay time the output current is limited by an internal current control loop.

### Power stages OUT7, OUT8, OUT15...OUT18:

In case of overload or short-circuit to Ubatt the current is limited and the corresponding bit combination is set (early warning) after a given delay time. They will not be turned off. If this condition leads to an overtemperature condition, the output will be set into a low duty cycle PWM (selective thermal shut- down with restart) to prevent critical chip temperature.

There are 3 possibilities to turn the power stages on again:

- turn the power stage off and on, either via serial control (SPI) or via parallel control (input pin, except outputs OUT17 and OUT18) or by the PPM-bus (ms-bus) (except OUT8, OUT17, OUT18)
- applying a reset signal
- sending the instruction "DEL_DIA" by the SPI-interface

## Description power stages

The VDD-monitoring locks all power stages, except OUT8 for access by the IN8 input. OUT8 is locked by an extra threshold of 3V maximum.

## Diagnosis

For all low side switches the following failure modes can be detected:

- Short to UBatt: (SCB), can be detected when switches are turned on
- Short to ground: (SCG), can be detected when switches are turned off
- Open load: (OL) , can be detected when switches are turned off
- Overtemperature: (OT) , will only be detected when switches are turned on

The fault conditions SCB, SCG, OL and OT will not be stored until an integrated filtering time is expired. If, at one output, several errors occur in a sequence, always the last detected error will be stored (with filtering time). All fault conditions are encoded in two bits per switch and are stored in the corresponding SPI registers. Additionally there are two central diagnostic bits: One special bit for OT and one bit for fault occurance at any output.

The registers can be read out via SPI. After each read out cycle the registers have to be cleared by the DEL_DIA command.

## SPI-Interface:

The serial SPI-interface establishes a communication link between CJ945C and the systems microcontroller. CJ945C always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 5 MBaud.
Applying an active slave select signal at SS, CJ945C is selected by the SPI master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.
In case of inactive slave select signal (High) the data output SO goes into tristate.

## PPM- Bus Interface (µs- Bus Interface):

As default (after reset), the power stages OUT1...OUT16 are controlled by the SPI-interface.
Alternatively these outputs can be controlled either by the pins IN1...IN16 or by the PPM-bus interface (ms-bus interface). The bit “Bus-Multiplex” (BMUX) in the SPI register CONFIG determines parallel access (IN1 ... IN16) or PPM-bus (ms-bus) control. There is one exception: If BMUX is set to ‘0’ only the power-stages OUT1...OUT7 and OUT9...OUT15 are controlled by the PPM-bus (ms-bus). OUT8 is controlled only by IN8 or by the SPI-interface.

### Main features

- 16 data bits for each data-frame (at the pin FDA)
- 16 clock-pulses for each data-frame (at the pin FCL) as minimum.
- Clock frequency 0...20 MHz
- One sync -input (pin SSY) to latch the input data stream
- No error correction

## Maximum ratings

### 1.1 Definition of test conditions

The integrated circuit must not be destroyed if maximum ratings are reached. Every maximum rating is allowed to be reached, as far as no other maximum rating is exceeded.
Unless otherwise indicated all voltages are referred to GND (GND pins 1...8 connected to each other).
Positive current flows into the IC.

### 1.2 Thermal limits

| | |
|---|---|
| Operating temperature continuous | -40°C ≤ $T_J$ ≤ 175°C |
| Storage temperature | -55°C ≤ $T_C$ ≤ 125°C |
| Thermal resistance | $R_{thJC}$ ≤ 2.5 K/W |

### 1.3 Electrical limits

Limits must absolutely not be exceeded. By exceeding only one limit the integrated circuit might be destroyed.

| **Power supplies $U_{VDD}$ and $U_{UBatt}$** | |
|---|---|
| Static (without destruction) *) | -0.3V ≤ $U_{VDD}$ ≤ 36V<br>-0.3V ≤ $U_{UBatt}$ ≤ 37V |
| Dynamic (without destruction) for t < 10µs | -0.5V ≤ $U_{VDD}$ ≤ 36V<br>-0.5V ≤ $U_{UBatt}$ ≤ 40V |

*) $U_{VDD}$ > 5.5V is allowed only in case of error conditions!
Not suitable for continuous operation.

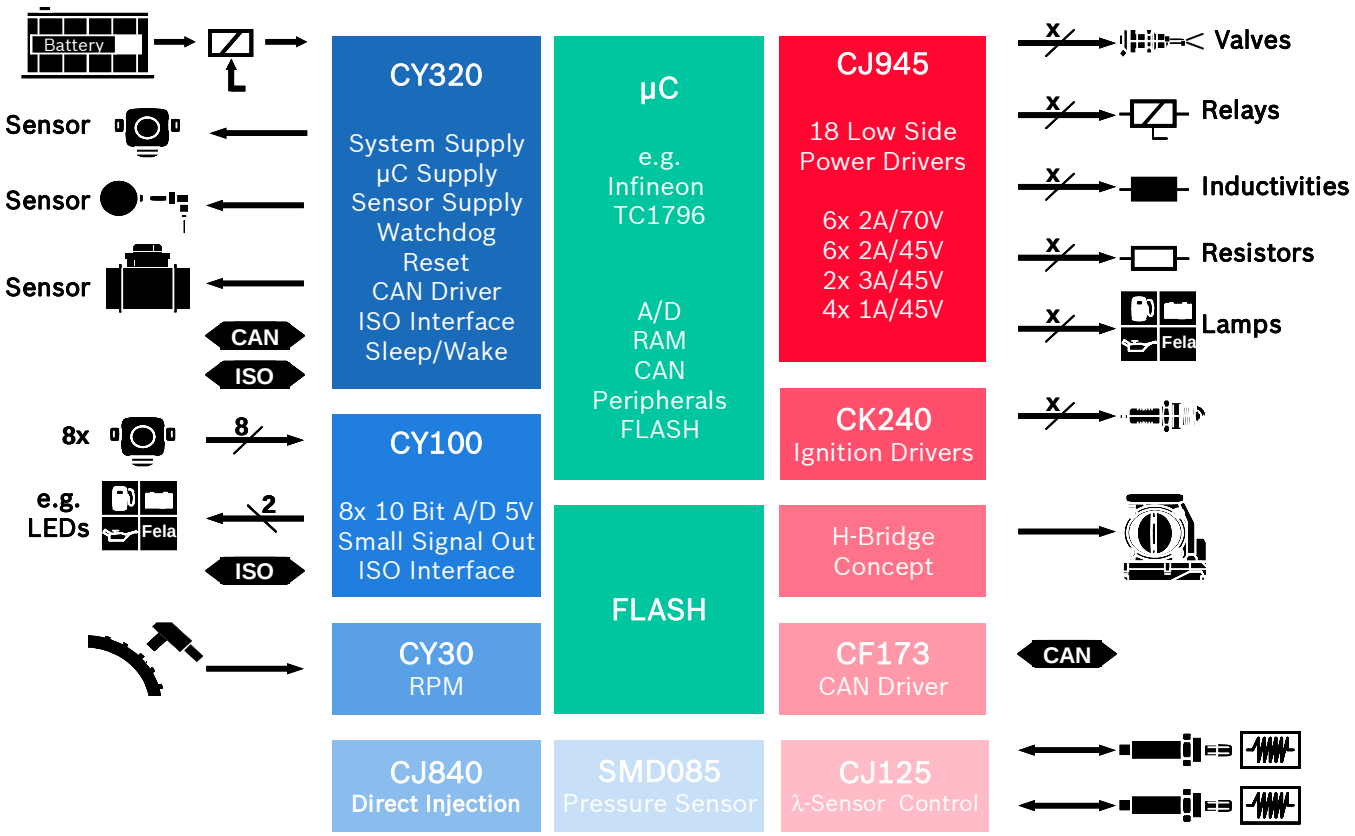
| **Outputs low side switches** | |
|---|---|
| Static voltage (without destruction)<br>- OUT1...OUT6<br>- OUT7...OUT18 | ≤ 64V<br>≤ 40V |
| Dynamic voltage without destruction after ISO/DIS7637-1, pulses 1 to 4<br>- OUT1 to OUT6, OUT9 to OUT16: via external load (e.g. 2W lamp)<br>- OUT7, OUT8, OUT17 and OUT18: via external load | <br><br>≤ 2ms<br><br>≤ 2ms |

| **Ground current** | |
|---|---|
| Total current GND1+2 (total ground current of OUT5, 6, 9, 10, 17, 18) | $I_{GND1+2}$ ≤ 18 A |
| Total current GND3+4 (total ground current of OUT1, 2, 7, 8, 11, 12, 15, 16) | $I_{GND3+4}$ ≤ 20 A |
| Total current GND5+6 (total ground current of OUT3, OUT13) | $I_{GND5+6}$ ≤ 6 A |
| Total current GND7+8 (total ground current of OUT4, OUT14) | $I_{GND7+8}$ ≤ 6 A |

Attention:
Even if all ground pins are connected with each other on the PCB the total ground currents $I_{GND1+2}$ and $I_{GND3+4}$ and $I_{GND5+6}$ and $I_{GND7+8}$ must not be exceeded.
The 4 ground pins GND1...4 are internally connected to the heat sink via an unspecified rivet joint. Therefore it is advisable to short-circuit the 4 ground pins on the PCB and to connect them with the heat sink. In addition the 4 ground pins GND5..8 must be connected to the other ground pins on the PCB.

| **Inputs of the power switches, SPI inputs, reset and shut-off of the power stages** | |
|---|---|
| Input voltage | -0.3V ≤ $U_{INi,RST,SS,SI,SCK,ABE}$ ≤ 7V |
| Input current | -100mA ≤ $I_{INi,RST}$ ≤ 5mA<br>-50mA ≤ $I_{SS,SI,SCK}$ ≤ -10mA<br>-100mA ≤ $I_{ABE}$ ≤ -20mA |
| **Pin RST** | |
| Minimum reset duration (Power-On) | 15 ms |
| **SPI output** | |
| Output voltage | -0.3V ≤ $U_{SO}$ ≤7V |
| Output current | $I_{SO}$ ≤ 5mA |

## Chipset





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