High Speed USB Platform Design Guidelines

Rev. 1.0

REVISION HISTORY

Revision	Revision History	Date
0.9	Preliminary release.	07/12/2000

Table of Contents:

1 Introduction

This document provides guidelines for integrating a discrete high speed USB host controller onto a four-layer desktop motherboard. The material covered can be broken into three main categories: Board design guidelines, EMI/ESD guidelines and front panel USB guidelines. Section 1.1 Background provides an explanation of the routing experiments and testing performed to validate the feasibility of 480 Megabits per second on an actual motherboard. Section 7 contains a design checklist that lists each design recommendation described in this document. High speed USB operation is described in the USB 2.0 Specification (http://www.usb.org/developers/docs.html).

Board design guidelines
Specific requirements concerning routing and placement of the host controller recommended trace separation, termination placement requirements and overall trace length guidelines are provided. These are followed by general guidelines concerning plane splits, layer stackup and component placement. Some examples of common routing mistakes are also included to show the designer some suggestions about what to avoid when routing USB signals.

EMI/ESD guidelines
EMI and ESD solutions are provided based on actual motherboard testing.

Front panel USB guidelines
Recommendations are made for front panel cabling, motherboard mating connector pin-out, routing considerations and daughterboard design guidelines. These guidelines are based on simulations as well as experimental testing and measurement.

1.1 Background

A variety of placement and routing options were investigated using high speed USB test silicon placed on a four-layer motherboard. This testing was performed to determine the feasibility of routing 480 Megabits per second high speed USB signals on a real motherboard using normal component placement, densities and routing constraints.

The Constraints
The routing of the Processor/Memory bus and PCI buses with today's chipsets does not leave many degrees of freedom for other motherboard signals as shown in Figure 1.

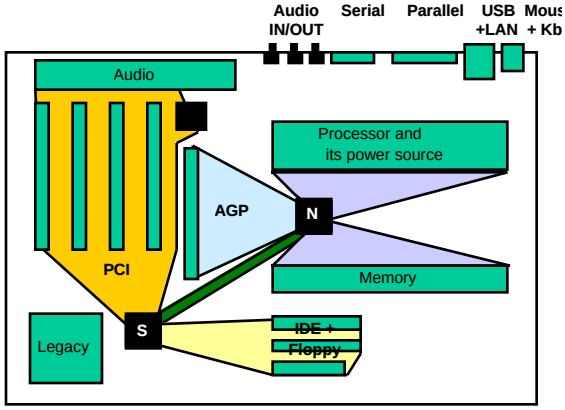
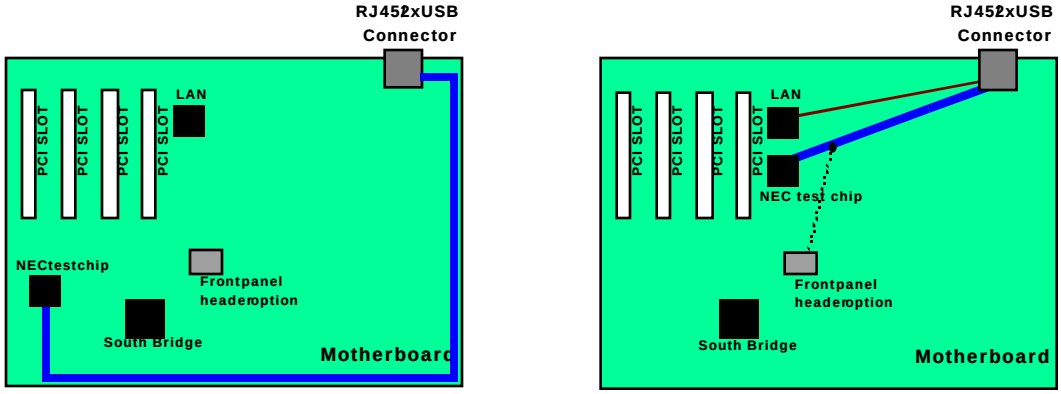


Figure 1 Major buses on current motherboards

A high speed USB host controller will attach to the PCI bus, and signals must be routed to the USB connectors. The high speed USB validation motherboard examined two candidate placement positions and two routing scenarios, as shown in Figure 2. The long route was chosen to use the path currently used by

most motherboards. The short route was chosen for comparison of routing lengths and via counts as well as proximity to high-speed interfaces like AGP. Both routes included common mode choke stuffing options near the USB back panel connectors to examine the effectiveness of possible EMI and ESD solutions. Some designs will additionally require front/side panel mount USB connectors, and this is typically implemented with 0.1-inch center stake pins and a front panel cable.



Long Route Short Route

Figure 2 Motherboard placement and routing options

The Results

Signal quality measurements, impedance measurements and EMI/ESD testing were performed using both routing scenarios to investigate the effects of vias, trace length, component placement and routing paths. Both routing scenarios passed all testing.

Conclusion

By following the guidelines in this document, either placement location should produce a successful high-speed USB-ready motherboard.

2 Terminology

Clock- Any periodic signal (as defined for EMC purposes) above 10MHz.

PCB- Printed circuit board

EMC- Electromagnetic Compatibility-The condition which prevails when electronic equipment/systems are collectively performing their individually designed functions in a common electromagnetic environment without causing or suffering unacceptable degradation due to EMI to or from other electronic equipment/systems in the same environment. EMC can be broken down to two major subcategories, emissions and immunity, with ESD being a subcategory of immunity.

EMI- Electromagnetic Interference-The opposite condition of EMC in which a piece of ITE causes or suffers unacceptable degradation to or from other electronic equipment in the same environment.

ESD- Electrostatic discharge

HS- High speed- USB signaling at 480 Mega bits per second

FS- Full speed- USB signaling at 12 Mega bits per second

3 Layout Guidelines

3.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The high speed USB validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

1. Place the high-speed USB host controller and major components on the unrouted board first.
2. With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
3. Route high-speed USB signals on bottom whenever possible.
4. Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
5. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
6. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
7. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.
8. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 3.6 Plane Splits, Voids and Cut-Outs (Anti-Etch) for more details on plane splits.
9. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
10. Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
11. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stackup the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

3.2 High Speed USB Trace Spacing

Use the following separation guidelines. Figure 3 provides an illustration of the recommended trace spacing.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used. For the board stackup parameters referred to in section 3.7 Layer Stacking, 7.5-mil traces with 7.5-mil spacing results in approximately 90 ohms differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

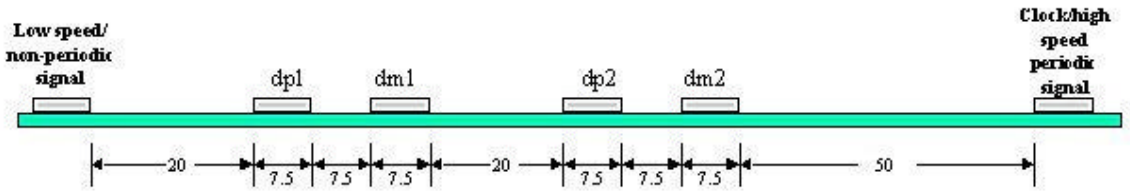


Figure 3 Recommended trace spacing (mils) for the stackup given in Section 3.7

3.3 High Speed USB Termination

Use the following termination guidelines.

1. High-speed USB designs require parallel termination at both the transmitter and receiver. For host controller designs that use external termination resistors, place the termination resistors as close as possible to the host controller signal pins. Recommend less than 200 mils if possible. Follow the manufacturer's recommendation for the termination value needed to obtain the required 45 ohm-to-ground parallel HS termination.
2. For downstream ports, a 15 kΩ pull down resistor on the connector side of the termination is required for device connection detection purposes. Note that this pull down might be integrated into the host controller silicon. Follow the manufacturer's recommendation for the specific part used.
3. A common mode (CM) choke should be used to terminate the high speed USB bus if they are need to pass EMI testing. Place the CM choke as close as possible to the connector pins. See Section 5.1 for details.

Note: Common mode chokes degrade signal quality, thus they should only be used if EMI is a known problem.

3.4 High Speed USB Trace Length Matching

Use the following trace length matching guidelines.

High-speed USB signal pair traces should be trace-length matched. Max trace-length mismatch between High-speed USB signal pairs (such as, DM1 and DP1) should be no greater than 150 mils.

3.5 High Speed USB Trace Length Guidelines

Use the following trace length guidelines.

Table 1 Trace length guidelines

Configuration	Trace Length	Cable Length	Total Length
Motherboard Back Panel	≤ 18 inches	NA	≤ 18 inches
Front panel①	≤ 6 inches (counting connector card trace length)	≤ 12 inches	≤ 18 inches

①see front panel design guidelines in Section 6 for more details.

3.6 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits, voids and cutouts.

VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

1. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clocks and signal traces as well as slower signal traces, which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)
2. Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to VCC5 and the other side should tie to VCC3. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guideline for the GND plane.

Avoid anti-etch on the GND plane.

3.7 Layer Stacking

The following guidelines apply to PCB stack-up.

Four-layer Stack-Up

1. Signal 1 (top)
2. VCC
3. GND
4. Signal 2 (bottom, best layer for USB2)

The high speed USB validation motherboard used 7.5-mil traces with 7.5-mil spacing between differential pairs to obtain 90Ω differential impedance. The specific board stackup used is as follows:

- 1 ounce copper
- prepreg 4.5 mils
- core 53 mils
- board thickness 63 mils
- ε_r 4.5

3.8 Component Placement

The following guidelines apply to component placement on the PCB.

1. Locate high current devices near the source of power and away from any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors.) This reduces the length that the return current travels and the amount of coupling to traces that are leaving the PCB.
2. Keep clock synthesizers, clock buffers, crystals and oscillators away from the high speed USB host controller, high speed USB traces, I/O ports, PCB edges, front panel headers, power connector, plane splits and mounting holes. This reduces the amount of radiation that can couple to the USB traces and other areas of the PCB.
3. Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple vias connecting to the ground plane. These will help reduce emissions.

4 Some Common Routing Mistakes

4.1 Stubs

A very common routing mistake is shown in **Figure 4**. Here the CAD designer could have avoided creating unnecessary stubs by proper placement of the pull down resistors over the path of the data traces. Once again, if a stub is unavoidable in the design, no stub should be greater than 200 mils.

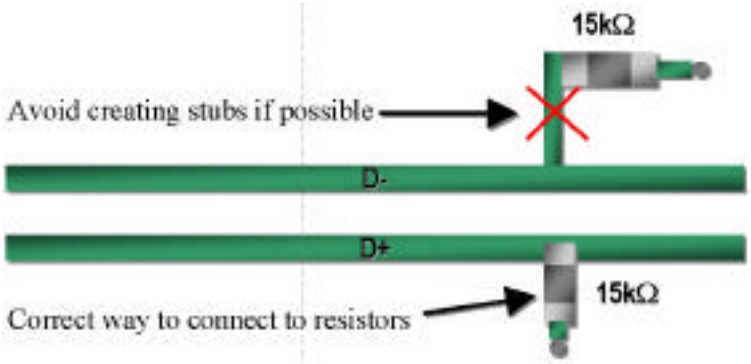


Figure 4 Creating unnecessary stubs

4.2 Poor Routing Techniques

Figure 5 demonstrates several violations of good routing practices for proper impedance control and signal quality of high speed USB signaling.

Crossing a plane split
The mistake shown here is where the data lines cross a plane split. This causes unpredictable return path currents and would likely cause a signal quality failure as well as creating EMI problems.

Creating a stub with a test point
Here is another example where a stub is created that could have been avoided. Stubs typically cause degradation of signal quality and can also affect EMI.

Failure to maintain parallelism
Figure 5 is also a classic example of a case where parallelism was not maintained, when it could have been. The red trace (the lighter trace farthest to the right with the "x" on it) shows the wrong way to route to the connector pins. The green trace (the darker trace in the middle) shows the correct way. Failing to maintain

parallelism will cause impedance discontinuities that will directly affect signal quality. In this case it also contributes to the trace-length mismatch and will cause an increase in signal skew.

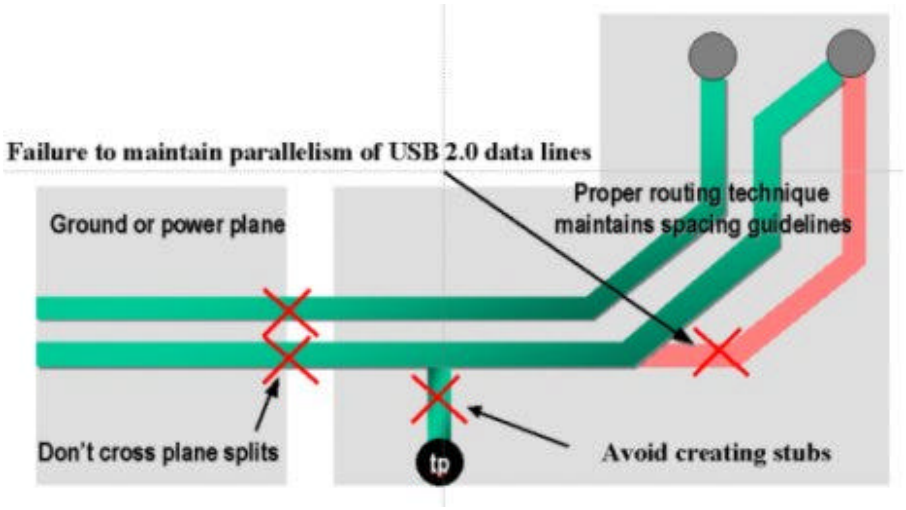


Figure 5 Violation of proper routing techniques

5 EMI/ESD Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

5.1 EMI - Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Figure 6 shows the schematic of a typical common mode choke and ESD suppression components (refer to Section 5.2 ESD
). The choke should be placed as close as possible to the USB connector signal pins.

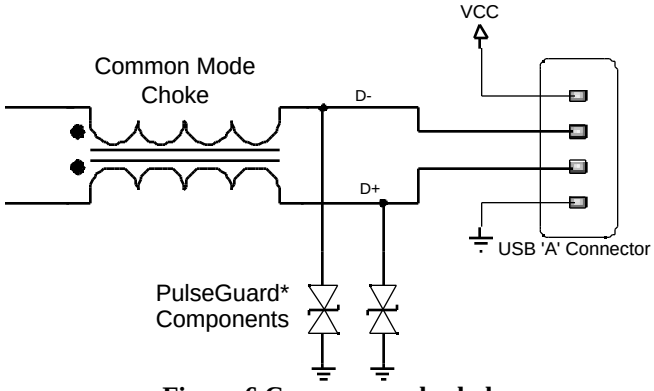
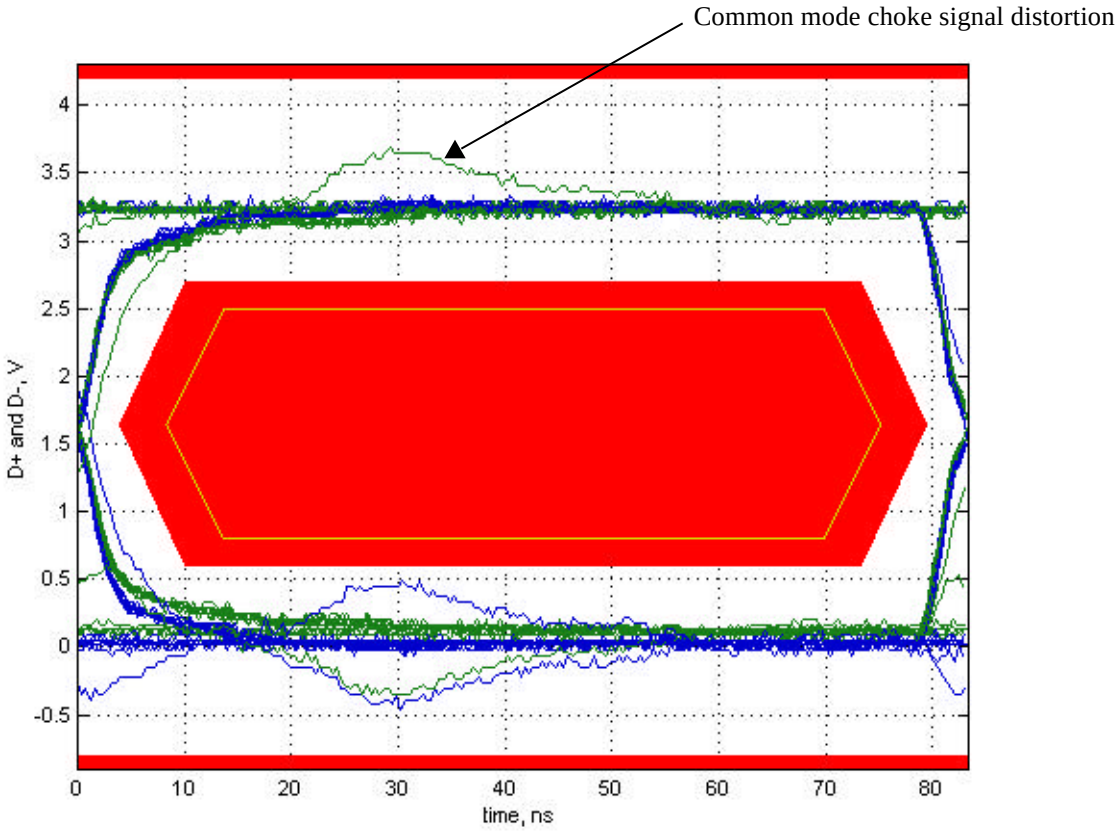


Figure 6 Common mode choke

Examples of specific common mode chokes that were tested for signal quality and EMI with passing results are given in Table 2. Other vendors make similar parts that may provide the same results but due to limited time and resources they were not tested.

Table 2 Common mode choke testing results

Vendor	MFN	Signal Quality Results	EMI Results
TDK	ACM2012-800-2P (90 ohm)	pass	not tested
TDK	ACM2520-201-2P (300 ohm)	pass	not tested
TDK	ACM3225-800-2P	pass	not tested
TDK	ACM3225-161-2P	pass	not tested
TDK	ACM2012-900-2P (90 ohm)	pass	not tested
Murata	plw3216s900sq2t1	pass	Pass
Murata	dln213900pg	pass	not tested



USB High Speed Signaling through a TDK ACM2012-900-2P Common Mode Choke

Common mode chokes distort full speed and high-speed signal quality. The eye diagram above shows full speed signal quality distortion of the end of packet, but still within the specification. As the common mode impedance increases, this distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that the designer is trying to suppress.
2. Once the designer has a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so be careful about increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low speed, Full speed and High speed USB operation.

5.2 ESD

Low-speed and full-speed USB provide ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique doesn't work for high speed USB due to the much higher signal rate of HS data. A device that has been tested successfully is based on spark gap technology. The specific device tested is a LittelFuse component, PulseGuard* PGB0010603 (0603 package size). Proper placement of the device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 6. Other low-capacitance ESD protection devices may work as well, but due to time and resource constraints none were investigated. As with the common mode choke solution, we recommend including the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing.

ESD protection and common mode chokes are only needed if the design does not pass EMI or ESD testing. Footprints for common mode chokes and/or ESD suppression components should be included in the event that a problem occurs(General routing and placement guidelines should be followed).

6 Front Panel Solutions

6.1 Cables

If multiple ports are required, the front panel cable solution chosen must meet all the requirements in Chapter 6 of the *USB 2.0 Specification* for High-/full-speed cabling for each port with the exceptions described in "Cable Option 2", below

.

6.1.1 Cable Option 1

Use standard HS/FS compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document. Examples of specific front panel cables were tested for impedance and are given in Table 2. Other vendors make similar parts that may provide the same results, but due to limited time and resources they were not tested.

Vendor	Part Number	Zmin	Zmax
Bizlink	750890-001	88.39	91.25
GreatLink	8004629	87.0	94.00
Greatlink	8004588	86.5	96.5
Foxconn	750890-001	74.5	80.0

6.1.2 Cable Option 2

Use custom cables that meet all of the requirements in Chapter 6 of the *USB 2.0 Specification* with the following additions/exceptions.

1. They can share a common jacket, shield and drain wire.

2. Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:

   2.1 The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughterboard). Refer to the front panel daughterboard referenced later for details.

Selecting proper wire size. A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 Specification* that has ≤ one-half the resistance of either of the two wires being combined. The data is provided for reference:

Table 3 Conductor Resistances

American Wire Gauge (AWG)	2 Ohms (Ω)/ 100 meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: 2 – 24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector since droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case all transients will be seen/damped by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See Section 7.2.2 and Section 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

An effort is currently underway to develop a front panel cable specification that meets the requirements described above. When complete, the cable specification will be added to this document as an update.

6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

6.2.1 Pin-out

A ten pin, 0.1-inch pitch stake pin assembly is recommended, with the pin-out listed in Table 4 and schematic shown in Figure 7.

Table 4. Front panel header pin-out

Pin	Description
1	Vcc
2	Vcc

3	dm1
4	dp1
5	dm2
6	dp2
7	Gnd
8	Gnd
9	Key
10	no-connect or over-current sense

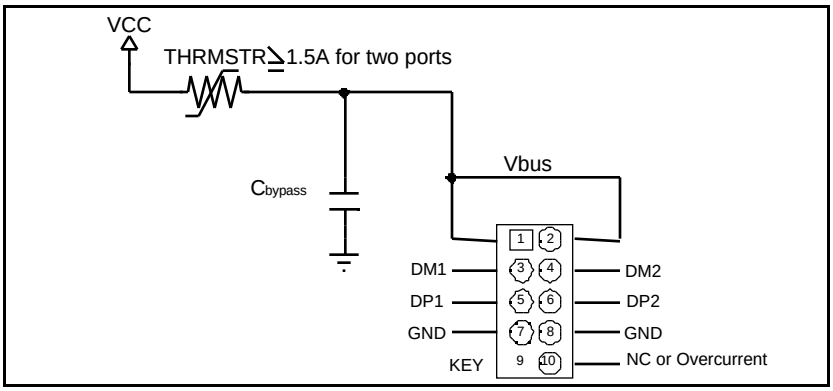


Figure 7 Front Panel Header Schematic

It is recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to prevent damage to the motherboard. This should be implemented only if the front panel solution does not apply a connector card that includes overcurrent protection.

1. This protects the motherboard from damage in the case where an unfused front panel cable solution is used.
2. It also provides protection from damage if an unkeyed cable is inadvertently plugged onto the front panel USB connector.
3. It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

6.2.2 Routing Considerations

1. Traces or surface shapes from VCC to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.

2. There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 8 shows the major components associated with a typical front/side panel USB solution that uses a front-panel connector card. Figure 9 shows a specific front-panel header solution that was used for the high speed USB motherboard validation experiment.

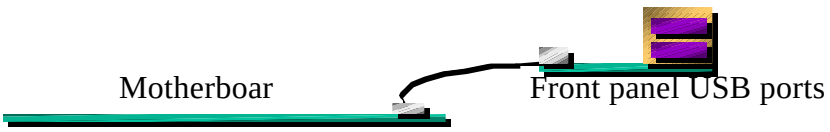


Figure 8 Motherboard front panel USB support

front panel cable

front panel connector card

Figure 9 Cable and connector card

Note: The terms “connector card” and “daughterboard” are used interchangeably.
When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren’t duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

6.3.1 Front panel daughterboard design guidelines

1. Place the Vbus bypass capacitance, CM choke and ESD suppression components on the daughterboard as close as possible to the connector pins.
2. Follow the same layout, routing and impedance control guidelines as specified for motherboards in Section 3 Layout Guidelines.
3. Minimize the trace length on the front panel connector card. Less than 1-inch trace length is recommended.
4. Use the same mating connector pin-out as outlined for the motherboard in Section 6.2.1 Pin-out.
5. Front panel trace length guidelines, as follows:

Use the following trace length guidelines for front panel USB support.

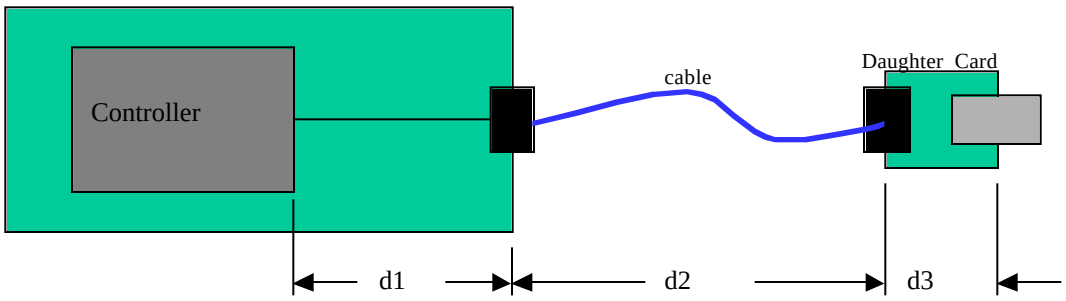


Figure 10 Front panel trace length guidelines

Total trace length = d1 + d2 + d3
The following maximum lengths are recommended for each segment:

Total trace length ≤ 18 inches
d1 (controller to front panel connector trace length) ≤ 5 inches
d2 (cable length) ≤ 12 inches
d3 (connector card trace length) ≤ 1 inch

Note that keeping the total length of both cabling and traces under the maximum recommended length is the actual target. The specific length targets for d1, d2 and d3 listed above are recommendations to meet this requirement. If the cable is shorter the trace lengths could be longer and vice versa.

7 High Speed USB Design Checklist

3.1 General Routing and Placement

	Item	Description
❑	1	Place the high-speed USB host controller and major components on the unrouted board first.
❑	2	With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
❑	3	Route high-speed USB signals on bottom whenever possible.
❑	4	Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
❑	5	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
❑	6	Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
❑	7	Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.
❑	8	Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical.
❑	9	Route USB trace pairs together.
❑	10	~~9.~~12. Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
❑	11	Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stackup the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

3.2 High Speed USB Trace Spacing

	Item	Description
❑	1	Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance.
❑	2	Verify with an impedance calculator that trace spacing and trace width used on the specific board stackup results in 90 ohms differential impedance.
❑	3	Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
❑	4	Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

3.3 3.3 High Speed USB Termination

	Item	Description
❑	1	If the host controller uses external termination resistors, verify that it is less than 200 mils from the HS output pins of the host controller.
❑	2	For downstream ports, verify that the 15k Ohm pull down resistors are between the termination resistors and the USB connector pins. Note that this pull down might be integrated into the host controller silicon. Follow the manufacturer's recommendation for the specific part used.
❑	3	A common mode (CM) choke should be used to terminate the high speed USB bus if they are need to pass EMI testing. Place the CM choke as close as possible to the connector pins. See Section 5.1 for details.

3.4 3.4 High Speed USB Trace Length Matching

	Item	Description
❑	1	HIGH SPEED USB signal pair traces should be trace length matched. Max trace length mismatch between HIGH SPEED USB signal pairs (such as, DM1 and DP1) should be no greater than 200 mils.

3.5 High Speed USB Trace Length Guidelines

	Item	Description
❑	1	Verify that the total high speed USB trace length to the back panel connectors is ≤ 18 inches
❑	2	Verify that the total trace and cable length to front panel USB connectors is ≤ 18 inches. This includes the trace length on the front panel connector card if present.

3.6 Plane Splits, Voids and Cut-Outs (Anti-Etch)

	Item	Description
❑	1	Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clocks and signal traces as well as slower signal traces, which might be coupling to them.
❑	2	Verify that no high-speed USB traces are routed within 25 mils of any plane splits.

3.8 Component Placement

	Item	Description
❑	1	Locate high current devices near the source of power and away from any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors.) This reduces the length that the return current travels and the amount of coupling to traces that are leaving the PCB..
❑	2	Keep clock synthesizers, clock buffers, crystals and oscillators away from the high speed USB host controller, high speed USB traces, I/O ports, PCB edges, front panel headers, power connector, plane splits and mounting holes. This reduces the amount of radiation that can couple to the USB traces and other areas of the PCB.
❑	3	Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple vias connecting to the ground plane. These will help reduce emissions.

6.1 Cables

	Item	Description
❑	1	If using standard USB HS/FS cables for front panel support ensure they meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*.
❑	2	If custom cables are used, verify the requirements of Section **Error! Reference source not found.** of this design guideline are followed.

6.2 Motherboard/PCB Mating Connector

	Item	Description
❑	1	Verify that the motherboard mating connector has the standard pin-out described in Section 6.2.1 Pin-out
❑	2	For front panel motherboard mating connectors, verify the routing considerations of Section 6.2.2 Routing Considerations are met.

6.3 Front Panel Connector Card

	Item	Description
❑	1	Place the Vbus bypass capacitance, CM choke and ESD suppression components on the daughterboard as close as possible to the connector pins.
❑	2	Follow the same layout, routing and impedance control guidelines as specified for motherboards in Section 3 Layout Guidelines.
❑	2	Minimize the trace length on the front panel connector card. Less than 1-inch trace length is recommended.
❑	4	Use the same mating connector pin-out as outlined for the motherboard in Section 6.2.1 Pin-out.